TRANSISTOR HAVING A HETEROJUNCTION AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to Chinese Patent Application No. 201410073625.0 filed on Mar. 3, 2014, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

Technical Field

The present disclosure generally relates to a transistor and a manufacturing method thereof. More particularly, the present disclosure relates to a transistor having a wide bandgap emitter and a manufacturing method thereof.

Description of the Related Art

As semiconductor technology advances, there is a need to develop more high-performance transistors in CMOS (Complementary Metal-Oxide-Semiconductor) fabrication process.

FIG. **1** illustrates a conventional transistor structure. As shown in FIG. **1**, the conventional transistor may include an N-well (NW) and a P-well (PW) formed in a semiconductor substrate. An emitter and a base are formed on the N-well, and a collector is formed on the P-well. The emitter, base, and collector are spaced apart from each by an insulating material disposed therebetween. In the example of FIG. **1**, an ion implantation process is performed on the regions corresponding to the emitter and the collector, so as to form a P+ region. Similarly, an ion implantation process is performed on the region corresponding to the base, so as to form an N+ region.

However, the conventional transistor of FIG. **1** does not provide superior performance, and therefore is unable to meet current semiconductor technology needs.

SUMMARY

The present disclosure addresses some of the deficiencies in conventional transistor structures.

According to some embodiments of the inventive concept, a transistor is provided. The transistor includes a semiconductor substrate comprising a first region and a second region; an emitter and a base disposed on the first region; and a collector disposed on the second region.

In some embodiments, the first region may be doped with an n-type impurity and the second region may be doped with a p-type impurity, the base may be doped with the n-type impurity, and a concentration of the n-type impurity in the base may be higher than a concentration of the n-type impurity in the first region.

In some embodiments, the collector may be doped with the p-type impurity, and a concentration of the p-type impurity in the collector may be higher than a concentration of the p-type impurity in the second region.

In some embodiments, the base may include phosphorous-doped silicon carbide and the emitter may include boron-doped silicon germanium.

In some embodiments, the collector may include the boron-doped silicon germanium.

In some embodiments, the first region may be doped with a p-type impurity and the second region may be doped with an n-type impurity, the base may be doped with the p-type impurity, and a concentration of the p-type impurity in the base may be higher than a concentration of the p-type impurity in the first region.

In some embodiments, the collector may be doped with the n-type impurity, and a concentration of the n-type impurity in the collector may be higher than a concentration of the n-type impurity in the second region.

In some embodiments, the emitter may include phosphorous-doped silicon carbide.

In some embodiments, the first region may be doped with a p-type impurity and the second region may be doped with an n-type impurity; and the emitter may include boron-doped silicon germanium.

In some embodiments, the base may include phosphorous-doped silicon carbide.

In some embodiments, the collector may include the boron-doped silicon germanium.

According to some other embodiments of the inventive concept, a method of manufacturing a transistor is provided. The method includes forming a first region and a second region on a semiconductor substrate; forming an emitter on the first region and a collector on the second region; and forming a base on the first region.

In some embodiments, the first region may be doped with an n-type impurity and the second region may be doped with a p-type impurity, the base may be doped with the n-type impurity, and a concentration of the n-type impurity in the base may be higher than a concentration of the n-type impurity in the first region.

In some embodiments, the collector may be doped with the p-type impurity, and a concentration of the p-type impurity in the collector may be higher than a concentration of the p-type impurity in the second region.

In some embodiments, the base may include phosphorous-doped silicon carbide, and the collector and the emitter may include boron-doped silicon germanium.

In some embodiments, the first region may be doped with a p-type impurity and the second region may be doped with an n-type impurity; and the emitter may include phosphorus-doped silicon carbide.

In some embodiments, the base may be doped with the p-type impurity, and a concentration of the p-type impurity in the base may be higher than a concentration of the p-type impurity in the first region.

In some embodiments, the collector may be doped with the n-type impurity, and a concentration of the n-type impurity in the collector may be higher than a concentration of the n-type impurity in the second region.

According to some further embodiments of the inventive concept, a method of manufacturing a transistor is provided. The method includes forming a first region and a second region on a semiconductor substrate, wherein the first region is doped with a p-type impurity and the second region is doped with an n-type impurity; forming an emitter on the first region and a collector on the second region, wherein the emitter includes boron-doped silicon germanium; and forming a base on the first region.

In some embodiments, the base may include phosphorous-doped silicon carbide and the collector may include the boron-doped silicon germanium.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated herein and constitute a part of the specification, illustrate different embodiments of the inventive concept and,